Embedded computing platforms require to support complex functionalities with high computational throughput. They must be able to execute challenging applications like the software-defined radio that aims to support numerous telecommunication standards on a single programmable platform. Beside those throughput and programmability requirements, embedded systems are highly constrained by power consumption. It is for example the case for battery-operated cell phones handsets or for their communication base stations which have cooling issues. Technology shrink still provides higher transistor count at each technology node but unfortunately, deep submicron nodes do not provide significant power improvements with scaling as in the previous decades. This leads to conflicting constraints of higher computation throughput in less power budget with limited technology improvements.

The approach followed in this work is to use homogeneous multicores that are easily programmable and scalable. In order to meet the embedded platforms constraints, the problem that needs to be addressed is to have a fully programmable processor core that can exploit instruction-level parallelism with a very high power efficiency and efficient inter-core communication support.

The main contribution of this thesis is a scalable processor architecture and execution model made of independent execution tiles. It uses an original dataflow execution engine to efficiently communicate data inside and between cores with synchronization capability. The execution model uses an original two-level code organization that allows to take benefit of loop locality even in case of complex control paths. Precise performances evaluations and comparisons are made on complete microarchitecture implementations of state-of-the-art embedded architecture models.