Ultra Low-Power design techniques

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Introduction
Battery-operated systems increasingly require ultra low-power (ULP) dissipation ICs. When reducing the supply voltage (V_{DD}) to achieve low-power (<100nW), threshold voltages V_t must be scaled as well to maintain speed performance. That causes leakage currents to increase exponentially, resulting in possibly dominant static power dissipation in such conditions. We propose a new ULP diode with transistors biased in very weak inversion regime in reverse mode. This diode can be used to realize memorization circuits and charge pumps with strongly reduced power dissipation.

Ultra-Low Leakage Diode
The reverse current of classical MOS diodes (i.e. a MOSFET with drain connected to gate) is equal to the MOS current I_s at V_{gs}=0V (fig.1), which becomes much higher than the junction leakage current for low V_t. We propose a new Ultra Low-Power diode (i.e. ULPD, combining a nMOS and a pMOSFET, fig.1) [1,2] that strongly reduces reverse current. When the diode is reversely biased by some hundred of mVs, the transistors operate with negative V_{gs} and the reverse current tends to the junction leakage current. ULPD allowed us to realize high-efficiency charge pumps for low power applications with high temperature functionality.

Memory cell

A novel ULP latch is obtained by connecting two reverse biased ULP diodes in series (fig. 2a). Two stable states appear, at “0” and “V_{DD}”, in the plot of the measured current difference between the lower and the upper ULPD (D2 and D1) versus the voltage level at the memory node (V_x) (fig. 2b). Subsequently, when a V_x between 0 and V_{DD}/2 (resp. V_{DD}/2 and V_{DD}) is imposed and then left floating, I_{D2-I_{D1}} is positive (resp. negative) and eventually drives V_x to “0” (resp. V_{DD}). Such architecture is therefore auto-regenerative for both logical levels “0” and “1”.

The ULP latch allows to realize SRAM cells with ultra low static consumption. In a stable logic state, the transistors of our cell are biased with low V_{ds} and negative gate to source voltages (V_{gs}) in very weak inversion, while V_{ds} is high and the minimum V_{gs} is 0 in a standard SRAM cell. This leads to an ultra low static consumption in comparison with standard SRAM. Memory cells realized on our 2µm Fully Depleted SOI technology presented a static current equal to the junction leakage (defined as the minimum drain to source current for negative gate to source voltage, \sim 10^{-14}A at room temperature). Good characteristics were observed up to 280°C, with very low static current (\sim 2.8 \times 10^{-14}A at 150°C; \sim 1.75 \times 10^{-13}A at 280°C), which ensures high temperature functionality.

Ultra-low static power consumption of the ULP latch allows also to realize level-keepers in MTCMOS circuits where floating nodes appear when circuit is in standby mode.

Related publications

![Figure 1. Standard and ULP MOS diode architectures and simulated I-V characteristics.](image1)

![Figure 2. Architecture and measured characteristic of an ULP memory with W=9.2µm and L=2µm under V_{DD}=0.5V.](image2)