Ultra-Low Power High-Temperature Voltage Reference Using Standard SOI CMOS Process

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We propose in this work a new principle of voltage reference for ultra-low power (ULP) applications. Such ULP source can be implemented on standard partially-depleted (PD) or fully-depleted (FD) SOI CMOS process, only requiring optimisation of the photo-lithographic masks definition in order to generate CMOSFETs with specific threshold voltages.

Multi-threshold voltages on standard SOI CMOS process

In standard CMOS process, n- and p-MOSFETs threshold voltages are usually set symmetrical in order to reduce the static consumption in digital circuits. The symmetry of these thresholds is the result of two different channel implantations. The way to obtain other threshold voltages is to switch the channel doping between n- and p-MOSFETs. Another possibility is to mask n- and p-MOSFETs during both channel implantation steps, in order to keep intrinsic (i.e. slightly P type in practice) channels. In some cases, both doping types can even be added. Figure 1 represents simulated Id-Vg curves (log scale) obtained from all possible combinations of channel masks in our FD-SOI CMOS process. In practice, special care is required with masks in order to avoid edge-effects in new devices. Note that some of these new devices are not suited for short channel operation (DIBL,…).

ULP Voltage reference principle

Figure 2 depicts the new ULP voltage reference architecture. The voltage reference value and temperature dependence depends on both transistors sizes and channel doping levels. This value can be extracted from the voltage corresponding to the intersection of n- and p-MOS Id-Vg curves of figure 1 (with a little correction due to substrate effects). This intersection also gives the circuit current consumption. For n- and p-MOSFETs with same channel doping and size at room temperature, the consumption is typically about a few picoamps only! When the temperature increases, the current consumption increases (but still remains very low) while the output voltage remains fairly constant. This is depicted in figure 3 and 4 in case of intrinsic n- and p-MOSFETs in our FD-SOI CMOS process. It can be shown that intrinsic devices present better matching properties when compared to doped devices, which makes them best candidates for precise voltage reference.

Publications:
  - Patent Application EP00870313.4